CLAIMS

1. A deblocking filter arithmetic apparatus comprising:

a first to an eighth arithmetic blocks which receive respectively, as inputs, simultaneously every two adjacent data among a first to an eighth pixel data, carry out one of the cycles of the processing arithmetic constituting the filtering processing corresponding to first to eighth pixel data and performed for removal of block noises, every time when two of the pixel data are input, and output the respective pixel data having been subjected to the filtering processing, being provided in parallel corresponding to the first to the eighth pixel data and to which two of the pixel data are input simultaneously;

an output selection circuit which selects one from the outputs from the first to the eighth arithmetic blocks and outputs the same; and

a control circuit which controls the processing arithmetic of each arithmetic block, in accordance with the cycles of the processing arithmetic, so that the cycles of the processing arithmetic performed in each combination, among a combination of the first and the second arithmetic block, a combination of the third and the fourth arithmetic block, a combination of the fifth

and the sixth arithmetic block, and a combination of the seventh and the eighth arithmetic block, respectively constituted by above-described arithmetic blocks up to the conclusion of the respective filtering processing should be the same and, further that the filtering processing of each combination should be concluded in an order successively among the respective combinations, and which controls the output selection circuit so as to select the output from the arithmetic blocks in a unit of the combination of the arithmetic blocks and to perform a pipeline output.

2. A deblocking filter arithmetic apparatus as defined in claim 1

wherein, the arithmetic block comprises

a first selection circuit which selects, according to the cycle of the processing arithmetic, any one among one of two pixel data input simultaneously, two values obtained respectively from the first pixel data and the eighth pixel data, and pixel data which are adjacent at outside the first pixel data and the eighth pixel data respectively, and value 0,

a second selection circuit which selects, according to the cycle of the processing arithmetic, any one among the other of two pixel data input simultaneously,

two values obtained respectively from the first pixel data and the eighth pixel data, and pixel data which are adjacent at outside the first pixel data and the eighth pixel data respectively, and value 0,

a third selection circuit which selects an arithmetic result for the accumulation or value 8,

a first shifter which receives, as input, the output of the first selection circuit,

a second shifter which receives, as input, the output of the second selection circuit,

an adder which adds together the output of the first shifter, the output of the second shifter and the output of the third selection circuit,

a register which receives, as input, the output of the adder and outputs the same as an arithmetic result for the accumulation to the third selection circuit, and

a third shifter which receives, as input, the output of the register and outputs the same as an arithmetic result to the output selection circuit.

3. A deblocking filter arithmetic method comprising:

a step for receiving, as inputs, simultaneously every two data among a first to an eighth successive pixel data and carrying out in parallel the processing arithmetic constituting the filtering processing

corresponding to the first to the eighth pixel data and performed for removal of block noises, so that the cycles of the processing arithmetic performed in each combination, among a combination of the first and the second arithmetic block, a combination of the third and the fourth arithmetic block, a combination of the fifth and the sixth arithmetic block, and a combination of the seventh and the eighth arithmetic block, respectively constituted by above-described arithmetic blocks up to the conclusion of the respective filtering processing should be the same and, further that the filtering processing of respective combinations should be concluded in an order successively, and

a step for performing a pipeline output of pixel data which are obtained by the above-described step with having been subjected to the filtering processing, for the respective combinations of the pixel data in an order successively.